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| 09/938,614 | 08/27/2001 | Hiroshi Kageyama | A8319.0004/P004 | 2342 |

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
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| 2673 | 4 |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/938,614 | KAGEYAMA ET AL. |
| | Examiner | Art Unit |
| | Leonid Shapiro | 2673 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-52* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

*Drawings*

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show T1-T2 in Fig. 2 as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

*Claim Objections*

2. Claim 19 objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 19 addresses positive and negative switching elements and is dependent on claims 8 and 4, which do not have positive and negative switching elements.

*Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3-8, 11-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear, what is the mining of the following: "a

plurality of variable resistor circuits which insert resistors....". Resistors could not insert resistors, switching elements could.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-20, 25-44 and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting (US Patent No. 5,952,948) in view of Jeong (US Patent No. 6,335,721 B1).

As to claim 1, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, in description See Col. 1, lines 38-49) each of which selects one of different reference voltages according to a digital gradation signal and inserts resistors with resistance values corresponding to the gradation signal into plurality of circuits connecting the selected reference voltages with an output terminal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20); the reference voltage selected by one of digital-to-analog conversion circuits and/or the reference voltage selected by the other of digital-to-analog conversion circuits are output to signal lines via the resistor inserted into any of circuits (See Figs. 4-5 items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which connects first output terminal to a plurality of signal lines one by one in response to a signal line selection signal synchronized with

gradation signal and connects second output terminal to a plurality of signal lines one by one in response to a signal line selection.

Jeong teaches a sampling circuit which connects first output terminal to a plurality of signal lines one by one in response to a signal line selection signal synchronized with gradation signal and connects second output terminal to a plurality of signal lines one by one in response to a signal line selection (See Figs. 2-3, items 30,64,66, in description See Col. 2, Lines 55-65 and Col.3, Lines 23-34). It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Jeong to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area (See Col. 2, Lines 57-58 in the Proebsting reference).

As to claim 2, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, in description See Col. 1, lines 38-49) each of which consists of plurality of switching elements with conduction resistances different from one another and connecting different reference voltages with an output terminal and in which specified switching elements conduct according to a digital gradation signal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20); wherein first group of sampling switching elements and second group of sampling switching elements start to conduct one by one in response to a signal line selection signal synchronized with gradation signal, and consequently the reference voltages connected to specified switching elements belonging to one of digital-to-analog conversion circuits and/or the reference voltages connected to specified switching elements belonging to the other of digital-to-analog conversion

circuits are output to signal lines via specified conducting switching elements (See Figs. 4-5 items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which has a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines and a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines

Jeong teaches a sampling circuit which has a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines and a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines (See Figs. 2-3, items 30,64,66, in description See Col. 2, Lines 55-65 and Col.3, Lines 23-34). It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Jeong to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area (See Col. 2, Lines 57-58 in the Proebsting reference).

As to claim 3, as best understood by the examiner, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, in description See Col. 1, lines 38-49) each of which selects one of different reference voltages according to a digital gradation signal and a plurality of **switching** (bolded by the examiner to show the difference with original claim) circuits which insert resistors with resistance values corresponding to gradation signal into a plurality of circuits connecting the reference voltages selected by digital-to-analog conversion circuits with an output terminal. (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20 wherein when sampling circuit selects signal lines, the reference voltage selected by one of digital-to-analog conversion

circuits and/or the reference voltage selected by the other of digital-to-analog conversion circuits are output to signal lines via resistor inserted into any of circuit (See Figs. 4-5 items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which connects first output terminal to a plurality of signal lines one by one in response to a signal line selection signal synchronized with gradation signal and connects second output terminal to a plurality of signal lines one by one in response to a signal line selection signal.

Jeong teaches a sampling circuit which connects first output terminal to a plurality of signal lines one by one in response to a signal line selection signal synchronized with gradation signal and connects second output terminal to a plurality of signal lines one by one in response to a signal line selection (See Figs. 2-3, items 30,64,66, in description See Col. 2, Lines 55-65 and Col.3, Lines 23-34). It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Jeong to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area (See Col. 2, Lines 57-58 in the Proebsting reference).

As to claim 4, as best understood by the examiner, Proebsting teaches a drive circuit, comprising: of plurality of **switching** (bolded by the examiner to show the difference with original claim) circuits insert resistors with resistors with resistance values corresponding to a digital gradation signal into plurality of circuits connecting one of plurality of digital-to-analog conversion circuits with an output terminal, plurality of digital-to-analog conversion circuits outputting an analog voltage by converting it into different reference voltage according to digital gradation signal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to

Col.5, Line 20); wherein first group of sampling switching elements and second group of sampling switching elements start to conduct one by one in response to a signal line selection signal synchronized with gradation signal and select the signal lines, and as a result of the signal line selection by sampling circuit, the reference voltages outputted from one of to one of digital-to-analog conversion circuits and/or the reference voltages outputted from the other of digital-to-analog conversion circuits are output to signal lines via the resistor inserted into any of circuits (See Figs. 4-5 items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which has a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines and a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines.

Jeong teaches a sampling circuit which has a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines and a first group of sampling switching elements inserted between first output terminal and a plurality of signal lines (See Figs. 2-3, items 30,64,66, in description See Col. 2, Lines 55-65 and Col.3, Lines 23-34). It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Jeong to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area (See Col. 2, Lines 57-58 in the Proebsting reference).

As to claims 5-8, as best understood by the examiner, Proebsting teaches switching elements which conduct according to gradation signal as the resistors values corresponding to gradation circuit and resistance elements, connected in series with each other, as the resistors

with resistance values corresponding to gradation signal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

As to claims 9-12, as best understood by the examiner, Proebsting and Jeong teach all limitations reflected in rejections of claims 1-4. The only difference between claims 1-4 and 9-12 positive and negative circuits.

Jeong teaches to generate negative and positive polarity video processor for converting the odd and even channel digital video signals outputted from the latch block into negative polarity analog video signals, and a switching block having plurality of switching circuits for receiving the negative and positive polarity analog video signals (See Figs. 4, 5, 7, in description See Col. 6, Lines 1-43 and Col. 7, lines 15-63). It would have been obvious to one of ordinary skill in the art at the time of invention to generate negative and positive polarity video processor for converting the odd and even channel digital video signals outputted from the latch block into negative polarity analog video signals, and a switching block having plurality of switching circuits for receiving the negative and positive polarity analog video signals as shown by Jeong to the Proebsting apparatus to generate positive and negative analog driving signals in order to satisfy the need for an LCD column driver circuit that consumes less power and area (See Col. 2, Lines 57-58 in the Proebsting reference).

As to claims 13-16, as best understood by the examiner, Proebsting teaches switching elements which conduct according to gradation signal as the resistors values corresponding to gradation circuit and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to gradation signal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

As to claims 17-18, Jeong teaches among the groups of the switching elements belonging to sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to signal line selection signal (See Fig. 3, items N-EN, Vdd1, in description See Col. 2, Lines 24-34).

As to claims 19-20, Jeong teaches among the groups of the positive switching elements belonging to positive sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to positive signal line selection signal and among the groups of the negative switching elements belonging to negative sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to negative signal line selection signal (See Figs. 1-3, items Channel, Row, N_EN, P_EN, OUTPUT, in description See from Col. 1, Line 16 to Col. 2, Line 34).

As to claims 25-32, 49-52, Proebsting teaching plurality of references voltages are fewer in numbers than the gradations of displayed images (See Figs. 3-5, items 300,302,206i,400,402, in description See from Col. 3, line 66 to Col. 4, Line9 and Lines 49-58).

As to claims 33-44, Proebsting teaching an image display apparatus with a drive circuit, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, an lector-optical conversion element or liquid crystal which changes its light transmittance or emission intensity to an electrical signal is placed near each intersection of the signal lines and scanning lines or liquid crystals are sandwiched between substrate and another substrate, signal lines are connected to drive circuit, and scanning line connected to a scanning circuit (See Fig.1, items 102-108, in description See Col. 1, Lines 5-65).

5. Claims 21-24, 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting and Jeong as aforementioned in claims 2,4,8,10,41-44 in view Nakamura et al. (US Patent no. 6,411,273 B1)

Proebsting and Jeong do not show switching elements are constituted of thin-film transistors.

Nakamura et al. teaches thin-film transistors as switching elements (See Fig. 14, items 117,117A, 118a, in description See Col. 45, Lines 11-16). It would have been obvious to one of ordinary skill in the art at the time of invention to use thin-film transistors as shown by Nakamura et al. in the Proebsting and Jeong apparatus in order to reduce power consumption (See Col. 2, Lines 54-59 in Nakamura et al. reference).

***Conclusion***

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kida et al. (US Patent No. 6,459,395 B1) reference discloses DAC and display unit with such DAC.

Chao et al. (US Patent No. 6,326,913 B1) reference discloses interpolating DAC and TFT-LCD driver using the same.

Kim et al. (US Patent No. 6,160,437) reference discloses Multiplexer for producing multi-level output signals.

Hamanishi et al. (US Patent No. 5,870,045) reference discloses D/A converter.

***Telephone inquire***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

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May 13, 2003

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